

**REMARKS**

Claims 1–23 are pending in the present application.

Claims 1–20 and 22–23 are allowed.

Claim 21 has been amended herein based upon the Examiner’s statement of reasons for allowance:

Claim 22–23 are allowed because the closed prior art of record fails to disclose a circuit as shown in Figure 2 wherein the edge counter comprises a sequence of logic gates between the input and an output that receive the input and produce the input and wherein a signal path between the input and output through the logic gates includes a sequence of only two logic gates . . .

Paper No. 20060717, page 3. Accordingly, the limitation “wherein a signal path between the input and output through the logic gates includes a sequence of only two logic gates” from claim 22 has been added to claim 21.

Allowance of the application is respectfully requested.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at [wmunck@munckbutrus.com](mailto:wmunck@munckbutrus.com).

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK BUTRUS, P.C.

Date:

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